REMARKS

In the present Office Action, claims 1-17 were pending before the Office. Of these claims 1, 7, 8, 16, and 17 were the only independent claims. The Office Action rejected claims 1-17.

Claims 10-15 and 17 were rejected under 35 U.S.C. § 112, first paragraph. Claims 4 and 9-15 were rejected under 35 U.S.C. § 112, second paragraph. Claims 1-3, 5-9, and 16 were rejected under 35 U.S.C. § 102(e). For at least the reasons set forth herein, these rejections are traversed and reconsideration is respectfully requested.

Claims 5 and 9-15 have been amended. No claims have been added, cancelled, or withdrawn.

A. ACCEPTANCE OF SUBMITTED DRAWINGS

In the Office Action, the Examiner indicates that the drawings submitted on December 21, 2003, are accepted. Applicants appreciate the indication that the drawings are accepted.

B. AMENDMENT TO THE DRAWINGS

Applicants submit herewith a replacement sheet for sheet 2 of the drawings. In FIG. 2, elements 206a-d have been corrected to NAND gates, rectifying a typographical error in the drawings submitted. Support for this change can be found throughout the Detailed Description and in claims 4 and 13. Thus, no new matter

has been entered.

C. REJECTION UNDER 35 U.S.C. § 112, FIRST PARAGRAPH

Claims 10-15 and 17 were rejected under 35 U.S.C. § 112, first paragraph as failing to comply with the enablement requirement. On page 2 of the Office Action, the Examiner asserts that "determine if only one of the input select signals is in the first logic state, and if so, output at least the select signal that is in the first logic state" as recited in instant claim 10 is not found in the specification. Applicants respectfully submit that support for this limitation is found, for example, at page 6, line 14, to page 7, line 15 of the specification where the SOSD circuit 114 and its operation are described. The specification at page 7, lines 9-15, summarizes that:

> Through use of the SOSD circuit 114, erroneous enabling of multiple clock signals via the multiplexer 102 is prevented, as only one select signal C1-C4 at a time may reach the multiplexer 102. Likewise, because each select signal C1-C4 is synchronized to a respective clock signal Clk_1-Clk_4, data paths through the multiplexer 102 are enabled/disabled in a substantially glitch-less manner.

The description that precedes the summary paragraph quoted above provides more than enough detail to enable one of ordinary skill in the art to "determine if only one of the input select signals is in the first logic state, and if so, output at least the select signal that is in the first logic state." Accordingly, Applicant respectfully requests reconsideration and

withdrawal of the rejection of claims 10-15 and 17.

D. REJECTION UNDER 35 U.S.C. § 112, SECOND PARAGRAPH

Claims 4 and 9-15 were rejected under 35 U.S.C. § 112, second paragraph, as being indefinite.

With regard to claim 4, the Examiner opines that a conflict exists between the limitation of "wherein preventing a first of the select signals that is in the first logic state from being provided to the multiplexer until the other select signals are in a second logic state" and the limitation of "performing a NAND operation on the first of the select signals and the NOR output," where the NOR output is from an intervening limitation. Applicant respectfully submits that a typographical error was made when drafting FIG. 2 in that elements 206a-d were incorrectly labeled as being AND gates when, in fact, elements 206a-d are described and claimed as being NAND gates, as the Examiner points out. Applicants submit herewith a replacement sheet 2 of drawings bearing a corrected FIG. 2 in which elements 206a-d are correctly labeled as being NAND gates. Support for this change can be found, for example, in claims 4 and 13 and in the specification at page 5, line 18, *et seq.* Accordingly, reconsideration and withdrawal of the rejection of claim 4 is respectfully requested.

With regard to claims 9-15, the Examiner states that there is no antecedent basis for "The apparatus" in the first line of each claim. While Applicants respectfully submit that one of

ordinary skill would recognize that "The apparatus" refers to the multiplexer system recited in independent apparatus claim 8, claims 9-15 have been amended to read --The multiplexer system-- at the beginning of each line to expedite prosecution.

E. REJECTION UNDER 35 U.S.C. § 102(e)

Claims 1-3, 5-9, and 16 stand rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,600,355 (*Nguyen*). The Examiner states that *Nguyen* discloses a multiplexer system (202) that receives input signals (CLK0, CLK90, CLK180, CLK270), has an output node (CKOUT) that outputs one of the input signals, has select nodes for respective input nodes that cause the multiplexer to select a different signal for output in response to a select signal of a first logic state being provided to the select node, and has selection circuitry (201) coupled to the multiplexer and adapted to prevent a select signal in a first logic state from being provided to the multiplexer until the other select signals are in a second logic state. For at least the following reasons, Applicants respectfully traverse this rejection.

Applicants respectfully submit that Nguyen does not disclose all limitations of, for example, instant claim 1. The select signals output by the state machine of *Nguyen* are provided to the multiplexer, as are the clock signals, but there is no prevention of a first of the select signals in a first logic state from being provided to the multiplexer until all other select signals are in a second logic state. All four select signals of

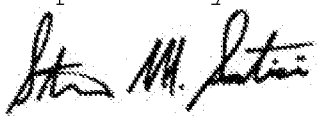
Nguyen are provided to the multiplexer of *Nguyen* regardless of their logic state. Similar arguments apply to claims 7, 8, 16, and 17. As noted in the application, this is prevented from happening so that if two or more select signals occupy a first logic state, no select signal is output to the multiplexer. Thus, since *Nguyen* does not disclose all of the limitations of, for example, instant claim 1, reconsideration and withdrawal of the rejection of claims 1-3, 5-9, and 16 are respectfully requested.

F. CONCLUSION

Since the Applicants assert that all the independent claims as amended are in condition for allowance and all remaining claims properly depend from the independent claims, Applicants assert that all claims are allowable.

Applicants do not believe a Request for Extension of Time is required but if it is, please accept this paragraph as a Request for Extension of Time and authorization to charge the requisite extension fee to Deposit Account No. 04-1696. Applicants do not believe any additional fees are due regarding this Amendment. However, if any additional fees are required, please charge Deposit Account No. 04-1696.

Respectfully Submitted,



Dated: January 2, 2008
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